

## PROFILE

- Embedded systems and networking software expert with over 20 years of experience architecting large systems with product teams of up to 60 people.
- Extensive experience porting both Linux and VxWorks to new platforms.
- Device driver for both Linux and VxWorks with both proprietary ASICs and vendor parts.
- Microcode for Intel and proprietary NPUs based on Tensilica cores.
- Extensive experience with the entire product cycle from scoping out market requirements, specifying functional requirements, design and architecture, and test plans.
- System software to handle system bring-up infrastructure, high availability frameworks.
- Extensive experience in datapath software in the networking and storage space.
- Experience designing debugging and post-mortem analysis tools, and working with hardware bring-up from initial stages.
- Represented companies at standards bodies, steering standard protocols toward better systems approaches and identifying market trends for new products.
- Proven experience with managing entire product cycle from product requirement definition, architecture and specification, design, implementation and prototyping to manufacturing.

## WORK EXPERIENCE

2008 – date      **Woven Systems, San Jose, CA**  
**Director of Platform Software**

Woven Systems is a startup involved with Ethernet switches for the data center with self-healing properties, congestion avoidance and low latency networks. Using an innovative technology invented in-house that works seamlessly with legacy networks, Woven switches interact with each other to build fabrics used for fast interconnect systems in cluster and grid computing.

- Architected and directed the development of a stable, reliable and high-available system from the prototype systems which were designed and implemented during the early startup stage.
- Implemented the software required to handle startup interaction in a large chassis based system for card interaction, configuration triggers, node and soft monitoring and life-cycle services.
- Analyzed multiple open-source embedded Linux build environment and modified one to existing platforms.
- Designed and implemented multiple debugging tools to support remote node debugging, in-system profiling, fault-isolation and post mortem analysis.
- Analyzed the commercial protocol software used on the switch product line and identified weak areas in the architecture.
- Led the architecture, design and implementation of AAA into the switch product line using TACACS+. Worked with a team of 6 engineers to implement this.
- Led the architecture, design and implementation of high availability software for the switch product line. Worked with a team of 8 engineers to implement the HA framework, and the soft APIs to be used by the application.
- Hired to develop distributed router to be built around Woven's fabric. This project was can-

celled to focus engineering resources to stabilize and harden existing system. Was kept on to lead this effort and ensure its success.

2006 – 2008 **Brocade Communications Systems, San Jose, CA**  
**Principal Software Architect**

Brocade Communications Systems is the industry leader in storage area networks. Principal software architect leading and defining requirements for a team of 60 engineers to define the high availability policy for switching solution of an integrated platform for both Data Center Ethernet and Fibre Channel.

- Architected the FCoE protocol design, its interaction with the translation ASIC that bridges FC and Ethernet switching domains. Implemented device drivers for FCoE ASIC against aggressive schedule.
- Architected the high availability framework for Brocade's new line of Data Center Ethernet Switches. This required significant deviation from Brocades existing mechanism to achieve acceptable switchover times. Involved in implementing the framework to support both state synchronization and event synchronization.
- Architected the data path micro-code and application AI for a multi-core TCP/IP network processor. Implemented a prototype iSCSI data model around this architecture that is used for existing iSCSI development.
- Supported the hardware team to debug the classifier, and TCP off-loader in the TOE. Implemented iSCSI CRC scheme to handle computations in real-time.
- Implemented various debugging tools such as kernel loggers, remote node debuggers and device driver analyzers to debug kernel device drivers.

2002 - 2006 **Integrated Device Technology, Santa Clara, CA**  
**Principal Engineer**

Integrated Device Technology is an industry leader involved in making integrated circuits for the networking equipment market. Principal engineer managing a team of 15 software engineers, actively involved in identifying strategic trends in networking products, architecting and defining new product lines for IDT.

- Represented IDT in the Network Processing Forum, an industry group of network semiconductor and equipment vendors defining a set of hardware-independent software APIs.
- Worked on five years strategic plan for wire-line networking equipment by researching this market segment to identify areas where IDT can create semiconductors.
- Implemented SystemC simulation of IDT's new classifier.
- Wrote micro-code to handle IPv4 LPM lookup using IDT's TCAM instead of software computation. Improved NPU core utilization by 225%.
- Wrote compiler to support Cisco CLI for ACLs and conversion of the ACLs for TCAM loading. Optimizations in compiler include minimization of re-arrangement, weight based database swapping.
- Worked on Intel NPU micro-code and interfaces for IDT's line of Network Search Engines (NSE), a line of ternary content addressable memories with enhanced support for networking applications, and invent software mechanisms to utilize these integrated circuits for longest prefix match route lookups, access control list filtering mechanisms etc.

1999 – 2002

## **Pluris, Cupertino, CA**

### **Lead Engineer**

Pluris was a late-stage startup involved in the design and manufacture of highly available terabit routers. These routers were large, scalable, distributed systems that spanned up to 128 chassis and were connected using an optical backplane. Responsible for the architecture of the software for overall system fault tolerance as well as fault tolerance in the MPLS protocol.

- Architected and implemented various system software components required to support redundancy on a highly available, distributed router. These modules implement software distribution and re-scheduling upon failover across multiple control hardware platforms, load balancing, and fault handling on a large distributed system.
- Invented a scheme for RSVP fault tolerance in the MPLS stack against an aggressive deadline.
- Designed debugging schemes to set breakpoints across a range of addresses/data on a PPC860 emulation platform, back-tracing of inter-task communications on a distributed platform, attach standard input and output to a subsidiary card using the system backplane.
- Implemented MPLS fast re-route for RSVP tunnels, traffic engineering database, SPF calculation and MPLS datapath drivers.
- Implemented VxWorks BSPs for a PPC 604 based line card and on PPC 860 emulation platforms. Wrote start-up code for the CPU, system controller and other peripheral devices on the board. Supported hardware teams with board bring-up.

1994 – 1999

## **Cabletron Systems, Santa Clara, CA**

### **Systems Architect**

Member of the start-up team of engineers in ZeitNet, a company specializing in ATM equipment, which got acquired by Cabletron Systems, and subsequently became Riverstone Networks.

- Lead the architecture and implementation of platform abstraction layers for ATM protocols to communicate in a portable fashion with switch fabric device drivers.
- Managed the architecture and implementation of fault tolerance for a 1+1 redundant system on the second generation ATM switch.
- Represented Zeitnet at the ATM Forum as well as IEEE 1394 Forum.
- Implemented switch fabric device drivers that programmed the ASICs to handle datapath switching, and set up QoS parameters for switches with capacities ranging from 2.5 GB to 10GB.
- Implemented VxWorks BSPs for two generations of switch hardware designed on the Intel i960 and MIPS R4000 processors and implemented drivers for the various switch fabric controllers. Wrote boot code, system initialization code and diagnostics for the CPU card.
- Firmware lead for the group of 5 engineers involved in designing an ATM uplink running on an intelligent controller with an Intel i960 to plug into an Ethernet switch backplane. This system would package the Ethernet packets from 32 10Mb duplex ports into two ATM OC-3 ports at line rate. This product was developed turnkey for Kalpana Networks, which was acquired by Cisco Systems.

1990 – 1994 **Cirrus Logic, Fremont, CA**

**Sr. Firmware Engineer**

- Architected and developed the framework to check the protocol conformance for the SCSI products of the mass storage group.
- Designed and implemented the caching scheme for mass storage devices to manage cache memory in an efficient fashion for disk accesses, thereby reducing seek and access times.
- Part of team defining a specialized instruction set for a storage controller to handle buffer management and SCSI protocol in an efficient fashion.
- Represented Cirrus Logic at SCSI standards meetings.

1988 – 1990 **Processor Systems, Bangalore, India**

**Design Engineer**

- Ported a TCP/IP and a PPP stack to an intelligent active hub without operating system support. Implemented a HDLC driver, a serial driver and the memory allocation mechanism to support the applications. This hub was designed to be a stand-alone box built around an Intel 80186 processor which could be managed in-band or out-of-band using PPP over a serial port.
- Designed and implemented the firmware for a caching SCSI disc controller running on an EISA bus. The firmware consisted of the SCSI state machine implementation, the caching sub-system, and a module to emulate the IDE interface so that the system could boot with an on-board BIOS.

**TECHNICAL SKILLS**

- Embedded system architecture and design on both Linux and VxWorks platforms.
- Fault tolerant and distributed system software design in large loosely distributed clusters.
- Extensive algorithm design
- Network processor and micro-code experience
- Extensive Protocol Implementation: MPLS, ATM, SCSI, IDE, 1394, FC, FCoE
- Ported VxWorks real-time operating system board support packages on multiple platforms
- Embedded kernel debugging tools, system diagnostic software and debug monitors
- Low-level microprocessor control and start-up (boot) code: PPC 604, PPC 860, MIPS R4000, Intel i960, Intel x86, Motorola 68000
- Extensive experience with device drivers
- Peripheral Devices: Custom ASICs, SCSI controllers (NCR 53C9x, 53C700), ATM SARs (NEC, TI), System Controllers (Galileo, PCI, Memory), Ethernet and serial controllers
- Expert in prototype bring-up and debugging
- Proficient in using Logic Analyzers and In-circuit Emulators for debugging systems

**EDUCATION**

1984 – 1988 **Birla Institute of Technology, Ranchi, India**

**BS, Electrical Engineering**